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(73) Patent Holder: 000005108
Hitachi, Ltd.
6, Surugadai 4-chome, Kanda, Chiyoda-ku, Tokyo

(72) Inventor: Shoji Shukuri
c/o Semiconductor Division, Hitachi, Ltd.
20-1, Josui-Honmachi 5-chome, Kodaira City, Tokyo

(72) Inventor: Rei Meguro
c/o Semiconductor Division, Hitachi, Ltd.
20-1, Josui-Honmachi 5-chome, Kodaira City, Tokyo

(72) Inventor: Ken'ichi Kuroda
c/o Semiconductor Division, Hitachi, Ltd.
20-1, Josui-Honmachi 5-chome, Kodaira City, Tokyo

(74) Agent: Patent attorney Yamato Tsutsui

Examiner: Asahi Shozan

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(54) [Title of the Invention] A semiconductor integrated circuit device and its manufacturing method

(57) [Scope of the Patent Claims]

[Claim 1]

A semiconductor integrated circuit where a nonvolatile memory cell is composed of MISFETs, and where a gate electrodes connected electrically to word lines are formed on a gate insulation film, formed on a first conductive type semiconductor substrate. The first and second semiconductor regions of the second conductive type comprising source and drain regions, are formed in the

semiconductor substrate, and a channel region is formed between the first semiconductor region and the second semiconductor region. The semiconductor integrated circuit device is characterized by the fact that the gate insulation film consists, at least in the first semiconductor region side, of three layers of insulation films where a silicon oxide film, a silicon nitride film, and the second silicon oxide film are accumulated, and that writing into the memory cell is performed by setting the second semiconductor region at a higher potential than the first semiconductor region.

[Claim 2]

A semiconductor integrated circuit where a nonvolatile memory cell is composed of MISFETs, and where the gate electrodes connected electrically to word lines are formed on a gate insulation film formed on a semiconductor substrate. The first and second semiconductor regions of the second conductive type comprising a source and a drain region are formed in the semiconductor substrate, and a channel region is formed between the first semiconductor region and the second semiconductor region. A semiconductor integrated circuit device characterized by the fact that the gate insulation film consists, at least in the first semiconductor region side, of three layers of insulation films where a silicon oxide film, a silicon nitride film, and a second silicon oxide film are accumulated, also that the impurity concentration in the part extending to the lower part of the gate electrodes in the first semiconductor region is lower than the impurity concentration in the part extending to the lower part of the gate electrodes in the second semiconductor region, and that hot electrons are injected to the silicon nitride film by generating the hot electrons in the first semiconductor region side.

[Claim 3]

A semiconductor integrated circuit where a nonvolatile memory cell is composed of MISFETs, and where the gate electrodes connected electrically to word lines are formed on a gate insulation film formed on a semiconductor substrate. The first and second semiconductor regions of the second conductive type comprising a source and drain regions are formed in the semiconductor substrate, and a channel region is formed between the first semiconductor region and the second semiconductor region. A semiconductor integrated circuit device characterized by the fact that the gate insulation film consists, in the first semiconductor region side, of three layers of insulation films where a silicon oxide film, a silicon nitride film, and a second silicon oxide film are accumulated. The second semiconductor region side consists of a silicon oxide film, and that the impurity concentration in the part extending to the lower part of the gate electrodes in the first semiconductor region is different from the impurity concentration in the part extending to the lower part of the gate electrodes in the second semiconductor region.

[Claim 4]

A semiconductor integrated circuit device described in Claim 1 or 3, characterized by the fact that the impurity concentration in the part extending to the lower part of the gate electrodes in the first semiconductor region is lower than the impurity concentration in the part extending to the lower part of the gate electrodes in the second semiconductor region.

[Claim 5]

A semiconductor integrated circuit device described in Claim 1, 2, or 4, characterized by the fact that the gate insulation film is made of three layers of insulation films comprising a first silicon oxide film, a silicon nitride film, and a second silicon oxide film are accumulated in the first semiconductor region side, and a silicon oxide film in the second semiconductor region side.

[Claim 6]

A semiconductor integrated circuit device described in one of the Claims 1~5, where a semiconductor integrated circuit device is characterized by the fact that the gate insulation film has the first semiconductor region side and the second semiconductor region side having almost the same electric capacity film thickness.

[Claim 7]

A semiconductor integrated circuit device described in Claim 1, 2, 4, 5, or 6, where a semiconductor integrated circuit device is characterized by the fact that the gate insulation film has the first semiconductor region side and the second semiconductor region side consisting of three layers of insulation films consisting of a first silicon oxide film, a silicon nitride film, and a second silicon oxide film are accumulated.

[Claim 8]

A semiconductor integrated circuit described in Claim 1, 3, 4, 5, 6, or 7, where a semiconductor integrated circuit device is characterized by the fact that writing into the memory cell is performed by injecting hot electrons into the silicon nitride film composing a part of the gate insulation film.

[Claim 9]

A semiconductor integrated circuit device described in one of the Claims 1~8, where a semiconductor integrated circuit device is characterized by the fact that among the three layers of insulation film composing at least a part of the gate insulation film, the film thickness of the first silicon oxide film formed in the lower layer of the silicon nitride film is thicker than the film thickness that direct tunnel current flows.

[Claim 10]

A semiconductor integrated circuit device described in one of the Claims 1~9, where a semiconductor integrated circuit device is characterized by the fact that the second semiconductor region consists of a first conductive type semiconductor region whose one end extends to the lower part of the gate electrodes and a second conductive type semiconductor region whose one end is separated from the gate electrodes, where the first semiconductor region is made of the second conductive type.

[Claim 11]

A semiconductor integrated circuit device described in one of the Claims 1~10, where a semiconductor integrated circuit device is characterized by the fact that reading out of the memory cell is performed by setting the first semiconductor region at higher potential than the second semiconductor region.

[Claim 12]

A semiconductor integrated circuit device described in one of the Claims 1~10, where a semiconductor integrated circuit device is characterized by the fact that reading out of the memory

cell is performed by setting the second semiconductor region at higher potential than the first semiconductor region.

[Claim 13]

A semiconductor integrated circuit device described in one of the Claims 1~12, where a semiconductor integrated circuit device is characterized by the fact that a source line is formed by a plug embedded in the first connection hole formed on the upper insulation film in one of the first and second semiconductor regions, and that bit lines are connected to the other of the first and second semiconductor regions via a plug embedded in the second connection hole formed on the insulation film in the upper part of the other of the first and second semiconductor regions.

[Claim 14]

A semiconductor integrated circuit device described in Claim 13, where a semiconductor integrated circuit device is characterized by the fact that the first connection hole and the second connection hole are formed self-aligned to the space of the gate electrodes of the MISFET.

[Claim 15]

A semiconductor integrated circuit device described in one of the Claims 1~14, where a semiconductor integrated circuit device is characterized by the fact that the memory cell consists of the MISFET comprising a memory element section and a selection MISFET.

[Claim 16]

A semiconductor integrated circuit device described in one of the Claims 1~9 and 11~15, where a semiconductor integrated circuit device is characterized by the fact that the first semiconductor region and the second semiconductor region are the same conductive type.

[Claim 17]

A semiconductor integrated circuit device manufacturing method characterized by the following processes:
(a) a process where, after forming the second silicon oxide film on a semiconductor substrate, the gate electrodes of MISFET are formed by patterning a conductor film formed on the top of the second silicon oxide film,
(b) a process where, after forming the second silicon nitride film on the semiconductor substrate containing the upper part of the gate electrodes, the fourth silicon oxide film is formed on the top of the second silicon nitride film,
(c) a process of exposing the upper part and side walls of the gate electrodes of the MISFET by etching the fourth silicon oxide film and the second silicon nitride film,
(d) a process of exposing the bottom face of the gate electrodes and the semiconductor substrate in the first region of the lower part of the gate electrodes and leaving the second silicon oxide film in the second region of the lower part of the gate electrodes by isotropically etching the second silicon oxide film,
(e) a process of forming the first silicon oxide film on the top face of the semiconductor substrate and the bottom face of the gate electrodes in the first region by thermally processing the semiconductor substrate, and

(f) a process of forming the second silicon nitride film on the semiconductor substrate containing a space between the first silicon oxide film formed on the top face of the semiconductor substrate and the first silicon oxide film formed on the bottom face of the gate electrodes in the first region.

[Claim 18]

Being a semiconductor integrated circuit device manufacturing method described in Claim 17, a semiconductor integrated circuit device manufacturing method characterized by the fact that it contains a process of introducing an self-aligned impurity to the end of the first region side of the gate electrodes to form the first semiconductor region in the semiconductor substrate and a process of introducing an self-aligned impurity to the end of the second region side of the gate electrodes to form the second semiconductor region in the semiconductor substrate, and that the impurity concentration in the first semiconductor region is set lower than the impurity concentration in the second semiconductor region.

[Claim 19]

Being a semiconductor integrated circuit device manufacturing method described in Claim 17 or 18, a semiconductor integrated circuit device manufacturing method characterized by the fact that the MISFET comprises a nonvolatile memory, that the gate electrodes of the MISFET comprising a peripheral circuit and the gate electrodes of the MISFET comprising the nonvolatile memory are formed in a process of patterning the same conductive film, and that the gate electrodes of the MISFET comprising the peripheral circuit are formed in a process of forming the second silicon oxide film.

[Detailed Explanation of the Invention]
[0001]
[Field of Technology]

This invention relates to a semiconductor integrated circuit device and its manufacturing technology, especially a technology effectively applicable to semiconductor integrated circuit devices which have a nonvolatile memory of the single MISFET structure that makes the insulation film trap a charge accumulation region.

[0002]
[Prior Art]

The basic cell structure of a nonvolatile memory formed on a silicon substrate is classified into two large categories: the floating gate type where a floating gate is installed between a gate oxide film and a control gate (word lines) above it and being electrically isolated from the surroundings is made a charge accumulation region, and an MNOS (Metal-gate Nitride Oxide Silicon) type where having no such floating gate, a gate insulation film is made of a cumulate film of a silicon oxide film and a silicon nitride film, and the electrons trapped in the silicon nitride film are made a charge accumulation region.

[0003]

Figure 52 is a cross-sectional view showing a representative cell structure of a floating gate type memory. This memory cell has a structure where a floating gate 103, an interlayer insulation film 104, and a control gate (CG) 105 are formed sequentially on the top of a gate oxide film 102 with a

film thickness of about 10 nm formed on the main surface of a silicon substrate 101, and a source (S) 106 and a drain (D) 107 are formed on the silicon substrate 101 on both sides of the floating gate 103.

[0004]

Writing into each memory cell is performed by injecting electrons 108 into the floating gate 103 and increasing the threshold voltage (Vth) of the transistor seen from the control gate 105 by 3V~5V compared with the condition where there is no accumulation of electrons 108. Also, the mainstream method of injecting electrons 108 into the floating gate 103 is to draw hot electrons generated by the avalanche breakdown near the drain 107 into the floating gate 103 by a positive voltage charged to the control gate 105.

[0005]

On the other hand, Fig. 53 is a cross-sectional view showing a representative cell structure of a MNOS-type memory cell. This memory cell consists of a MISFET (memory element section) where a silicon nitride film 113 and a writing/erasing gate electrode (PEG) 115a are formed sequentially on the top of a direct tunnel oxide film 112 with a film thickness of about 2 nm formed on the main surface of a silicon substrate 111 and a source (S) 116 and a connecting diffusion layer (drain) 117 are formed on the silicon substrate 111 on both sides of the gate electrode 115a. A selection MISFET where a selection gate electrode (SG) 115b on the top of the gate oxide film 118 is formed and a connecting diffusion layer (source) 117 and a drain (D) 119 are formed on the silicon substrate 111 on both sides of the gate electrode 115b.

[0006]

Writing into each memory cell is performed by increasing the threshold voltage of the MISFET in the memory element section through controlling the potential of the silicon substrate 111 and the writing/erasing gate electrode 115a to inject electrons 108 from the silicon substrate 111 side via the direct tunnel oxide film 112 onto the whole surface of the silicon nitride film 113 and make them trapped. Also, erasing is performed in the same way by decreasing the threshold voltage of the MISFET in the memory element section through controlling the potential of the silicon substrate 111 and the writing/erasing gate electrode 115a to eject electrons trapped in the silicon nitride film 113 to the silicon substrate 111 side. In this erasing operation, because the threshold voltage of the memory element section is lowered to below 0 V, namely down to the depression region, the selection MISFET becomes necessary other than the MISFET in the memory element section for reading out.

[0007]

Because the NMOS-type memory cell has an operation scheme of trapping electrons inside an insulation film (silicon nitride film 113), trapped electrons contribute to the modulation of the threshold voltage independently. Therefore, a variation of the threshold voltage over the entire channel region of the memory element section due to partial leakage of electrons inside the silicon nitride film 113 caused by defects inside the tunnel film 112 is very small. In other words, its retention property is excellent, and it can be to be a highly reliable memory cell scheme.

[0008]

Figure 54 is a cross-sectional view showing a cell structure named "Self-Aligned Split-Gate EEPROM Device" described in USP No. 5408115. This memory cell has a structure where a gate oxide film

122 and a selection gate electrode (SG) 123 are accumulated on the main surface of a silicon substrate 121. A side wall gate electrode (SWG) 127 is formed on those side walls via a three-layer insulation film consisting of a silicon oxide film 124, silicon nitride film 125, and a silicon oxide film 126. Also, a source (S) 128 is formed by ion injection masked with this side wall gate electrode (SWG) 127, and a drain (D) 129 is formed by ion injection masked with the selection gate electrode 123.

[0009]

As described in "1997 Symposium on VLSI Technology Digest of Technical Papers p63-p64", writing into a memory cell is performed by charging the source 128, side wall gate electrode 127, and selection gate electrode 123 with voltages of 5 V, 9 V, and 1 V, respectively with the drain 129 as the ground level.

[0010]

Figure 55 shows the potential distribution and electric field intensity distribution of the channel region in the writing operation of the memory cell. Because the voltage (5 V) charged between the source (S) and drain (D) is mostly charged to a void layer of the source, the electric field intensity along the channel direction becomes maximum immediately below the side wall gate electrode (SWG) as shown in the figure. Therefore, electrons running from the drain (D) to the channel region are accelerated in a high electric field region near the source (S) leading to the avalanche breakdown, and hot electrons generated at this time are injected and trapped in the silicon nitride film (125) by a vertical high electric field caused by the side wall gate electrode (SWG). Namely, by electrons being trapped in the silicon nitride film (125) immediately below the side wall gate electrode (SWG), the threshold voltage seen from the side wall gate electrode (SWG) rises up. The writing scheme by these hot electrons is basically identical to the scheme where the hot electrons near the drain in the floating gate type memory cell are drawing into the floating gate.

[0011]

Also, in reading out of the memory cell, a voltage of 1.8 V is charged to the side wall gate electrode (127) and the selection gate electrode (123) with the source (128) as the ground level, and modulation of the threshold voltage seen from the side wall gate electrode (127) due to presence/absence of an electron trap in the silicon nitride film (125) is judged from the drain current. Because this memory cell performs writing using hot electrons, even if the silicon oxide film (124) immediately below the silicon nitride film that traps the electrons is formed with a thicker film thickness (about 10 nm for example) than the direct tunnel oxide film of the MNOS-type memory cell, the writing speed does not become degraded. Also, the thicker this silicon oxide film (124) is, the lower the defect density becomes, and the retention property of the memory cell improves as the result.

[0012]

IEEE Electron Device Lett., (vol. EDL-8, no. 3, pp. 93-95, March 1987) discloses a nonvolatile memory of the single MISFET structure which has no control gate. Memory cell of this nonvolatile memory consist of a gate electrode of polycrystalline silicon formed on the top of a gate insulation film, with a source and a drain formed on a semiconductor substrate on both sides of this gate electrode, and the gate insulation film consists of the three-layer structure where a silicon nitride film is sandwiched between two layers of silicon oxide film.

[0013]

Writing into each memory cell is performed by making the carriers near the drain to be injected into the silicon nitride film and trapped. This memory cell is excellent in its retention property compared with the MNOS-type memory cell because the carriers in the silicon nitride film sandwiched by two layers of silicon oxide films exist locally in a narrow region near the drain.

[0014]

Japanese Patent Disclosure Hei 6-232416 public report discloses nonvolatile memory of the single MISFET structure where a gate insulation film and a trap film that retains the carriers are formed in sequence on the top of a channel region between a source and a drain, and a gate electrode is formed on the top of this gate insulation film and trap film. The gate insulation film is made of a silicon oxide film, and the trap film consists of a three-layer structure where a silicon nitride film is sandwiched between two layers of silicon oxide film.

[0015]

Writing into each memory cell is performed by injecting electrons into a silicon nitride film and trapping them in a silicon oxide film (tunnel oxide film) of a bottom layer comprising a part of the trap film. Because this memory cell forms a gate insulation film of a normal enhancement MISFET and a trap film in the memory section that retains the carriers in the lower part of a single gate electrode, the cell area can be reduced.

[0016]

[Problems Overcome by the Invention]

The floating gate type memory cell described above can be designed with relatively a small cell area because a control gate (word lines) is accumulated on the top of a floating gate, having a cell structure fit for increasing the capacity. On the other hand, although the MNOS-type memory cell has an excellent retention property compared with the floating gate type memory cell, being regarded as a highly reliable cell scheme, because it requires two basic elements for a memory element section and selection, the cell area under the same design rule becomes 4~5 times larger than the floating gate type memory cell, having the shortcoming of not being fit for increasing the capacity.

[0017]

Also, the memory cell disclosed in USP No. 5408115 has comparable scalability to the floating gate type memory cell and a reliability equivalent to or higher than the MNOS-type memory cell. However, its cell structure having a selection gate electrode and a side wall gate electrode makes the writing/erasing operation complicated compared with the floating gate type memory cell, increasing the required peripheral circuit area as the result. Moreover, because the side wall gate electrode is about 100 nm in width, its wiring resistance increases to 5~7 times as large as normal gate resistance, introducing degradation of the read-out speed. Furthermore, although the channel region between the selection gate electrode and the side wall gate electrode, namely immediately below the region where a silicon oxide film (124), a silicon nitride film (125), and a silicon oxide film (126) are accumulated in the horizontal direction is as small as about 30 nm in width, and the gate electrode

does not exist on its top. Therefore, this region functions as a parasitic resistance, causing a problem of decreasing the drain current at read-out and degrading the read-out speed.

[0018]

The objective of this invention is to provide a nonvolatile memory equipped with a new cell structure having both scalability comparable to the floating gate type memory cell and the reliability equivalent or higher than the MNOS-type memory cell and its manufacturing method.

[0019]

This and other objectives and new characteristics of this invention will become evident from the descriptions in this specification and attached drawings.

[0020]

[Problem Resolution Means]

Among the inventions disclosed in this application, outlines of the representative ones are explained as follows.

[0021]

In the nonvolatile memory cell in this invention, is composed of MISFETs where gate electrodes connected electrically to word lines are formed on a gate insulation film, formed on a first conductive type semiconductor substrate. The first and second semiconductor regions of the second conductive type comprising the source and drain regions are formed in the semiconductor substrate, and a channel region is formed between the first semiconductor region and the second semiconductor region. The gate insulation film consists, at least in the first semiconductor region side, of three layers of insulation films where the first silicon oxide film, a silicon nitride film, and the second silicon oxide film are accumulated.

[0022]

Writing into the memory cell is performed by setting the second semiconductor region at a higher electric level than the first semiconductor region in the selected memory cell and injecting hot electrons generated in the second conductive-type semiconductor region with a low impurity concentration into an electron trap in a silicon nitride film.

[0023]

Other than that, the inventions described in this application are explained item by item as follows.

[0024]

1. A semiconductor integrated circuit where a nonvolatile memory cell is composed of MISFETs, where the gate electrodes connected electrically to word lines are formed on a gate insulation film, formed on a first conductive type semiconductor substrate. The first and second semiconductor regions of the second conductive type comprising the source and drain regions are formed in the semiconductor substrate, and a channel region is formed between the first semiconductor region and

the second semiconductor region. A semiconductor integrated circuit device characterized by the fact that the gate insulation film consists, at least in the first semiconductor region side, of three layers of insulation films where a first silicon oxide film, a silicon nitride film, and the second silicon oxide film are accumulated, and that writing into the memory cell is performed by setting the second semiconductor region at a higher potential than the first semiconductor region.

[0025]

2. A semiconductor integrated circuit where a nonvolatile memory cell is composed of MISFETs where the gate electrodes connected electrically to word lines are formed on a gate insulation film, formed on a semiconductor substrate. The first and second semiconductor regions of the second conductive type comprising the source and drain regions are formed in the semiconductor substrate, and a channel region is formed between the first semiconductor region and the second semiconductor region. A semiconductor integrated circuit device characterized by the fact that the gate insulation film consists, at least in the first semiconductor region side, of three layers of insulation films where a first silicon oxide film, a silicon nitride film, and the second silicon oxide film are accumulated, that the impurity concentration in the part extending to the lower part of the gate electrodes in the first semiconductor region is lower than the impurity concentration in the part extending to the lower part of the gate electrodes in the second semiconductor region, and that hot electrons are injected to the silicon nitride film by generating the hot electrons in the first semiconductor region side.

[0026]

3. A semiconductor integrated circuit where a nonvolatile memory cell is composed of MISFETs where the gate electrodes connected electrically to word lines are formed on a gate insulation film formed on a semiconductor substrate. The first and second semiconductor regions of the second conductive type comprising the source and drain regions are formed in the semiconductor substrate, and a channel region is formed between the first semiconductor region and the second semiconductor region. A semiconductor integrated circuit device characterized by the fact that the gate insulation film consists, in the first semiconductor region side, of three layers of insulation films where the first silicon oxide film, a silicon nitride film, and the second silicon oxide film are accumulated, that the second semiconductor region side consists of a silicon oxide film, and that the impurity concentration in the part extending to the lower part of the gate electrodes in the first semiconductor region is different from the impurity concentration in the part extending to the lower part of the gate electrodes in the second semiconductor region.

[0027]

4. In Claim 1 or 3, a semiconductor integrated circuit device characterized by the fact that the impurity concentration in the part extending to the lower part of the gate electrodes in the first semiconductor region is lower than the impurity concentration in the part extending to the lower part of the gate electrodes in the second semiconductor region.

[0028]

5. In Claim 1, 2, or 4, a semiconductor integrated circuit device characterized by the fact that the gate insulation film is made of three layers of insulation films where the first silicon oxide film, silicon nitride film, and the second silicon oxide film are accumulated in the first semiconductor region side, and a silicon oxide film in the second semiconductor region side.

[0029]

6. In one of the Claims 1~5, a semiconductor integrated circuit device characterized by the fact that the gate insulation film has the first semiconductor region side and the second semiconductor region side having almost the same electric capacity film thickness.

[0030]

7. In Claim 1, 2, 4, 5, or 6, a semiconductor integrated circuit device characterized by the fact that the gate insulation film has the first semiconductor region side and the second semiconductor region side consisting of three layers of insulation films where the first silicon oxide film, silicon nitride film, and the second silicon oxide film are accumulated.

[0031]

8. In Claim 1, 3, 4, 5, 6, or 7, a semiconductor integrated circuit device characterized by the fact that writing into the memory cell is performed by injecting hot electrons into the silicon nitride film composing a part of the gate insulation film.

[0032]

9. In one of the Claims 1~8, a semiconductor integrated circuit device characterized by the fact that among the three layers of insulation film composing at least a part of the gate insulation film, the film thickness of the first silicon oxide film formed in the lower layer of the silicon nitride film is thicker than the film thickness that direct tunnel current flows.

[0033]

10. In one of the Claims 1~9, a semiconductor integrated circuit device characterized by the fact that the second semiconductor region consists of a first conductive type semiconductor region whose one end extends to the lower part of the gate electrodes and a second conductive type semiconductor region whose one end is separated from the gate electrodes, where the first semiconductor region is made of the second conductive type.

[0034]

11. In one of the Claims 1~10, a semiconductor integrated circuit device characterized by the fact that reading out of the memory cell is performed by setting the first semiconductor region at a higher potential than the second semiconductor region.

[0035]

12. In one of the Claims 1~10, a semiconductor integrated circuit device characterized by the fact that reading out of the memory cell is performed by setting the second semiconductor region at a higher potential than the first semiconductor region.

[0036]

13. In one of the Claims 1~12, a semiconductor integrated circuit device characterized by the fact that a source line is formed by a plug embedded in the first connection hole formed on the upper

insulation film in one of the first and second semiconductor regions, and that bit lines are connected to the other of the first and second semiconductor regions via a plug embedded in the second connection hole formed on the insulation film in the upper part of the other of the first and second semiconductor regions.

[0037]

14. In the Claim 13, a semiconductor integrated circuit device characterized by the fact that the first connection hole and the second connection hole are formed self-aligned to the space of the gate electrode of the MISFET.

[0038]

15. In one of the Claims 1~14, a semiconductor integrated circuit device characterized by the fact that the memory cell consists of the MISFET comprising a memory element section and a selection MISFET.

[0039]

16. In one of the Claims 1~9 and 11~15, a semiconductor integrated circuit device characterized by the fact that the first semiconductor region and the second semiconductor region are the same conductive type.

[0040]

17. A semiconductor integrated circuit device manufacturing method characterized by the following processes:
(a) a process where, after forming the first silicon oxide film on a semiconductor substrate, a silicon nitride film is formed on the first silicon oxide film, (b) a process where, by patterning the first silicon oxide film and the silicon nitride film, the first silicon oxide film and the silicon nitride film are left on the first region on the semiconductor substrate, and the first silicon oxide film and the silicon nitride film in the second region are removed, (c) a process of forming the second silicon oxide film on the top of the silicon nitride film in the first region on the semiconductor substrate and in the second region on the semiconductor substrate, and (d) a process where, by patterning a conductive film formed on the top of the second silicon oxide film, gate electrodes of MISFET is formed on the second silicon oxide film in the first and second regions.

[0041]

18. A semiconductor integrated circuit device manufacturing method characterized by the following processes:
(a) a process where, after forming the second silicon oxide film on a semiconductor substrate, the gate electrodes of MISFET are formed by patterning a conductor film formed on the top of the second silicon oxide film, (b) a process where, after forming the second silicon nitride film on the semiconductor substrate containing the upper part of the gate electrodes, the fourth silicon oxide film is formed on the top of the second silicon nitride film, (c) a process of exposing the upper part and side walls of the gate electrodes of the MISFET by etching the fourth silicon oxide film and the second silicon nitride film, (d) a process of exposing the bottom face of the gate electrodes and the semiconductor substrate in the first region of the lower part of the gate electrodes and leaving the second silicon oxide film in the second region of the lower part of the gate electrodes by isotropically

etching the second silicon oxide film, (e) a process of forming the first silicon oxide film on the top face of the semiconductor substrate and the bottom face of the gate electrodes in the first region by thermally processing the semiconductor substrate, and (f) a process of forming the second silicon nitride film on the semiconductor substrate containing a space between the first silicon oxide film formed on the top face of the semiconductor substrate and the first silicon oxide film formed on the bottom face of the gate electrodes in the first region.

[0042]

19. In Claim 17 or 18, a semiconductor integrated circuit device manufacturing method characterized by the fact that it contains a process of introducing an self-aligned impurity to the end of the first region side of the gate electrodes to form the first semiconductor region in the semiconductor substrate and a process of introducing an self-aligned impurity to the end of the second region side of the gate electrodes to form the second semiconductor region in the semiconductor substrate, and that the impurity concentration in the first semiconductor region is set lower than the impurity concentration in the second semiconductor region.

[0043]

20. In the Claim 17, 18, or 19, a semiconductor integrated circuit device manufacturing method characterized by the fact that the MISFET comprises nonvolatile memory, that gate electrodes of the MISFET comprising a peripheral circuit and gate electrodes of the MISFET comprising the nonvolatile memory are formed in a process of patterning the same conductive film, and that gate electrodes of the MISFET comprising the peripheral circuit are formed in a process of forming the second silicon oxide film.

[0044]

[Embodiments of the Invention]

Below, the embodiments of this invention are explained in detail based on the drawings. Here, in all the drawings for explaining the embodiments, the same code is used for the elements having the same function, and repetitions of the explanation are omitted.

[0045]

(Embodiment 1)

Figure 1 is an outline circuit diagram showing the main part of a flash memory (lump erasing type nonvolatile memory) which is an embodiment of this invention.

[0046]

In the memory cell array (MA) of this flash memory, are formed a plurality of word lines WL (WL1~WLm) and a plurality of source lines SL (SL1~SLm/2) extending in the right-left direction (X direction) of the figure, a plurality of bit lines DL (DL1~DLn) extending in the Y direction intersecting with them perpendicularly, and a plurality of memory cells M (M11~Mnm) configured in the MISFET structure described later.

[0047]

Each of the word lines WL (WL1~WLm) is connected to the gate electrodes of a plurality of memory cells, positioned along the X direction, and its one end is connected to a row decoder (X-DEC). Each of the source lines SL (SL1~SLm/2) is positioned as one between two word lines WL and is connected to a source common to two memory cells M neighboring in the Y direction. Also, one end of these source lines SL (SL1~SLm/2) is connected to a common source line CSL positioned in the peripheral part of the memory cell array (MA). Each of the bit lines DL (DL1~DLn) is connected to a drain common to two memory cells neighboring in the Y direction, and its one end is connected to a column decoder (Y-DEC) and a sense-up (SA).

[0048]

Figure 2 is a cross-sectional view of the main part of a semiconductor substrate showing a part of each of the memory cell array and the neighboring peripheral circuit. Fig. 3 (A) is a plan view showing a conductive layer pattern equivalent to about four memory cells, and Fig. 3 (B) is a plan view showing a conductive layer pattern equivalent to about 12 memory cells.

[0049]

A p-type well 5 is formed in a memory cell array region of a semiconductor substrate 1 made of a p-type silicon single crystal, and a p-type well 6 and an n-type well 6 are formed in the peripheral circuit region. Also, in the bottom part of the p-type well 5 in the memory cell array region, a deep n-type well 4 for separating electrically this p-type well 5 from the other regions of the semiconductor substrate is formed. On the surface of each of the p-type well 5 and the n-type well 6, is formed a field oxide film 2 made of a silicon oxide film for element separation.

[0050]

In the p-type well 5 in the memory cell array region, is formed an n-channel type MISFET Qm comprising a memory cell. Also, in the p-type well 5 in the peripheral circuit region, is formed an n-channel type MISFET Qn comprising a part of the peripheral circuit, and in the n-type well 6, is formed a p-channel type MISFET Qp comprising the other part of the peripheral circuit.

[0051]

The MISFET Qm comprising a memory cell consists mainly of a gate electrode 10a formed on a gate insulation film, an n^+-type semiconductor region 13 (drain) whose one end extends to the bottom of the gate electrode 10a, an n^+-type semiconductor region 15 (high concentration source) formed offset relative to the gate electrode 10a, an n^--type semiconductor region 11 (low concentration source) which is formed around the n^+-type semiconductor region 15 and whose one end extends to the bottom of the gate electrode 10a, and a channel formation region (p-type well 5) sandwiched by the source and drain. The gate electrode 10a is configured as one body with the word lines WL, and the source (n^+-type semiconductor region 15, n^-type semiconductor region 11) is configured as one body with the source lines SL.

[0052]

The gate electrode 10a consists of, for example, a polycide film where a W (tungsten) silicide film is accumulated on the top of an n-type polycrystalline silicon film, and on its side walls are formed a side wall spacer 16 composed of a silicon oxide film. Also, a gate insulation film formed on the

bottom of the gate electrode 10a consists of one layer of silicon oxide film 9 in the drain side and three layers of insulation films where a silicon oxid film 7 and a silicon nitride film 8 are accumulated on the bottom of the silicon oxide film 9 in the source side.

[0053]

The p-channel type MISFET Qp in the peripheral circuit consists mainly of a gate electrode 10b formed on a gate insulation film (silicon oxide film 9), a pair of n^+-type semiconductor regions 14 (source and drain) formed offset relative to the gate electrode 10b, a pair of p^--type semiconductor regions 12 whose one end extends to the bottom of the gate electrode 10b, and a channel formation region (p-type well 5) sandwiched by the source and drain. Also, the n-channel type MISFET Qn in the peripheral circuit consists mainly of a gate electrode 10c formed on a gate insulation film (silicon oxide film 9), a pair of n^+-type semiconductor regions 15 (source and drain) formed offset relative to the gate electrode 10c, a pair of n^--type semiconductor regions 11 whose one end extends to the bottom of the gate electrode 10c, and a channel formation region (p-type well 5) sandwiched by the source and drain. Namely, the p-channel type MISFET Qp and the n-channel type MISFET Qn in the peripheral circuit are configured with the LDD (Lightly Doped Drain) structure. The gate electrode 10b of the p-channel type MISFET Qp and the gate electrode 10c of the n-channel type MISFT Qn are composed of polycide film in the same way as the gate electrode 10a in the memory cell, and a side wall spacer 16 composed of a silicon oxide film is formed on their side walls.

[0054]

A silicon oxide film 17 with a thick film is formed on the top of the memory cell (MISFET Qm), p-channel type MISFET Qp, and n-channel type MISFET Qn, and on its top are formed wirings 23~27 composed of an Al alloy film for example.

[0055]

The wiring 23 formed on the memory cell array region comprises the bit lines DL and is connected to a drain (n^+-type semiconductor region 13) of the memory cell via a contact hole 20 formed on a silicon oxide film 17. Also, among the wirings 24~27 formed in the peripheral circuit region, the wirings 24 and 25 are connected to a pair of p^+-type semiconductor regions 14 (source and drain) of the p-channel type MISFET Qp via a pair of contact holes 21 formed on the silicon oxide film 17, and the wirings 26 and 27 are connected to a pair of n^+-type semiconductor regions 15 (source and drain) of the n-channel type MISFET Qn via a pair of contact holes 22 formed on the silicon oxide film 17.

[0056]

Next, the program operations of the flash memory are explained using Fig. 4 (an outline cross-sectional view showing about one memory cell), Fig. 5 (the memory cell operation voltage table), and Fig. 6 (a plot showing the potential distribution and electric field intensity distribution in the channel region at the writing operation of the memory cell).

[0057]

The writing operation sets the source (11, 15) of a selected memory cell (MISFET Qm) to the ground level (0 V) and charges the gate electrode (10a) and the drain (13) each with a positive voltage of 5 V. By this, a peak of electric field intensity shown in Fig. 6 occurs at the edge of the low concentration source (11), hot electrons (e^-) generated in this region (low concentration source side) are injected into

the electron trap inside the silicon nitride film 8, and the threshold voltage seen from the gate electrode (10a) rises, performing a writing operation.

[0058]

Also, the reading operation is performed in the same way by setting the source (11, 15) of a selected memory cell to the ground level (0 V) and charging the gate electrode (10a) and the drain (13) each with a positive voltage of 2 V. The erasing operation is performed by setting the drain (13) of a memory cell to the ground level (0 V), charging the source (11, 15) with a positive voltage of 5 V and the gate electrode (10) with a negative voltage of -10 V, respectively, and ejecting the electrons trapped in the silicon nitride film 8 to the substrate (p-type well 5) side, lowering the threshold voltage seen from the gate electrode (10a).

[0059]

Next, an example of the manufacturing method of the nonvolatile memory is explained using Fig. 7 ~ Fig. 18 (essential-section cross-sectional views of the semiconductor substrate each showing a part of the memory cell array region and its neighboring peripheral circuit region).

[0060]

First, a semiconductor substrate 1 made of a p-type silicon single crystal having a specific resistance of about 10 Ωcm is prepared as shown in Fig. 7, and after a field oxide film 2 with a film thickness of about 500 nm is formed on its surface by the selective oxidization (LOCOS) method, the semiconductor substrate 1 is thermally oxidized, forming a silicon oxide film 3 with a film thickness of about 20 nm on the surface of the element forming region surrounded with the filed oxide film 2. The silicon oxide film 3 is used as a mask when an impurity is ion implanted into the semiconductor substrate 1 in the next process.

[0061]

Next, as shown in Fig. 8, after forming a deep n-type well 4 on the semiconductor substrate 1 in the memory cell array region, a shallow p-type well 5 is formed on the semiconductor substrate 1 in the memory cell array region and a part of the peripheral circuit (n-channel type MISFET forming region), and a shallow n-type well 6 is formed on the semiconductor substrate 1 in the other part of the peripheral circuit (p-channel type MISFET forming region).

[0062]

The deep n-type well 4 is formed by ion-implanting the n-type impurity (phosphorus) to the semiconductor substrate 1 under a condition of acceleration energy 3000 keV and dose amount $1\times10^{13}/cm^2$ masked with a photoresist film with a film thickness of about 5 μm where an opening is installed in the memory cell array region. Also, the shallow p-type well 5 is formed by ion-implanting a p-type impurity (boron) to the semiconductor substrate 1 under a condition of acceleration energy 450 keV and dose amount $1\times10^{13}/cm^2$, and acceleration energy 2000 keV and dose amount $3\times10^{12}/cm^2$ masked with a photoresist film with a film thickness of about 2.5 μm where openings are installed in the memory cell array region and the n-channel type MISFET forming region. Moreover, the shallow n-type well 6 is formed by ion-implanting an n-type impurity (phosphorus) to the semiconductor substrate 1 under a condition of acceleration energy 1000 keV and dose amount $1.5\times10^{13}/cm^2$, acceleration energy 370 keV and dose amount $3\times10^{13}/cm^2$, and

acceleration energy 180 keV and dose amount $1\times10^{12}/cm^2$ masked with a photoresist film with a film thickness of about 2.5 μm where an opening is installed in the p-channel type MISFET forming region.

[0063]

Here, in the ion implantation process for forming the p-type well 5, an impurity (boron) for adjusting the threshold voltage (Vth) of the memory cell (MISFET Qm) and n-channel type MISFET Qn is ion injected at the same time (acceleration energy 50 keV, dose amount $1.2\times10^{12}/cm^2$). Also, in the ion implantation process for forming the n-type well 6, impurity (boron) for adjusting the threshold voltage (Vth) of the p-channel type MISFET Qp is ion injected at the same time (acceleration energy 20 keV, dose amount $1.5\times10^{12}/cm^2$).

[0064]

Next, after removing the silicon oxide film 3 on the surfaces of the p-type well 5 and the n-type well 6 by wet etching, as shown in Fig. 9, the semiconductor substrate 1 is thermally oxidized at about 750°C to form a silicon oxide film 7 with a film thickness of about 7 nm on the surfaces of the p-type well 5 and the n-type well 6, and further a silicon nitride film 8 with a film thickness of about 7 nm is accumulated on the top of the silicon oxide film 7 by the thermal CVD method at about 800°C.

[0065]

Next, as shown in Fig. 10, the silicon nitride film 8 and a silicon oxide film 7 are patterned to leave these films only in the source forming region of the memory cell and its vicinity. Patterning of the silicon nitride film 8 is performed by dry etching masked with a photoresist film with a film thickness of about 1 μm where openings are installed in the source forming region and its vicinity, and the patterning of the silicon oxide film 7 is performed by dry etching masked with the silicon nitride film 8 after removing the photoresist film by ashing. The widths of the two layers of insulation films (silicon oxide film 7 and silicon nitride film 8) left in the source forming region and its vicinity are adjusted so that the length of the lower portion of the gate electrode 10a (length of the longest dimension of the gate) formed in a later process becomes about 20 nm ~ 200 nm.

[0066]

Next, as shown in Fig. 11, the semiconductor substrate 1 is thermally oxidized at about 800°C to form a silicon oxide film 9 with a film thickness of about 15 nm on the surfaces of the p-type well 5 and the n-type well 6. At this time, because the silicon nitride film 8 in the memory cell array region is oxidized at the same time, a silicon oxide film 9 with a film thickness of about 2 nm is also formed on that surface.

[0067]

Next, as shown in Fig. 12, a gate electrode 10a of the memory cell (MISFET Qm) is formed on the silicon oxide film 9 in the memory cell array region, and a gate electrode 10b of the p-channel type MISFET Qn and a gate electrode 10c of the n-channel type MSFET Qp are formed on the silicon oxide film 9 in the peripheral circuit region. The gate electrodes 10a, 10b, and 10c are formed by accumulating a polycrystalline silicon film with a film thickness of about 100 nm and phosphorus concentration of about $2\times10^{20}/cm^3$ and a W silicide film with a film thickness of about 50 nm by the

thermal CVD method at about 600°C on the silicon oxide film 9, and then patterning these films by dry etching masked with a photoresist film.

[0068]

Next, as shown in Fig. 13, an n^--type semiconductor regions 11 with a low impurity concentration are formed on the p-type well 5 on both sides of each of the gate electrodes 10a and 10c and the n-type well 6 on both sides of the gate electrode 10b by ion-implanting n-type impurity (phosphorus) to the whole surface of the semiconductor substrate 1 under a condition of acceleration energy 40 keV and dose amount $1\times10^{13}/cm^2$.

[0069]

Next, as shown in Fig. 14, an n^+-type semiconductor region 13 comprising the drain of the memory cell is formed by ion-implanting an n-type impurity (arsenic) to the p-type well 5 masked with a photoresist film with a film thickness of about 1 μm where an opening is installed in the drain forming region of the memory cell under a condition of acceleration energy 50 keV and dose amount $3\times10^{15}/cm^2$.

[0070]

Next, as shown in Fig. 15, a p^--type semiconductor region 12 with a low impurity concentration is formed through compensating the n^--type semiconductor region 11 to the n-type well 6 on both sides of the gate electrode 10b by ion-implanting a p-type impurity (boron difluoride) to the n-type well 6 masked with a photoresist film with a film thickness of about 1 μm where an opening is installed in the p-channel type MISFET forming region under a condition of acceleration energy 50 keV and dose amount $2\times10^{13}/cm^2$.

[0071]

Next, as shown in Fig. 16, after accumulating a silicon oxide film (not shown in the figure) with a film thickness of about 200 nm on the semiconductor substrate 1 by the CVD method, a side wall spacer 16 of about 150 nm in width is formed on the side wall of each of the gate electrodes 10a, 10b, and 10c by etching anisotropically this silicon oxide film. At this time, the silicon oxide film 9 and the silicon nitride film 8 covering the source forming region of the memory cell are also etched.

[0072]

Next, as shown in Fig. 17, a p^+-type semiconductor region 14 with a high impurity concentraton comprising the source and drain of the p-channel type MISFET is formed by ion-implanting a p-type impurity (boron difluoride) to the n-type well 6 masked with a photoresist film with a film thickness of about 1 μm where an opening is installed in the p-channel type MISFET forming region under a condition of acceleration energy 50 keV and dose amount $3\times10^{15}/cm^2$.

[0073]

Subsequently, an n^+-type semiconductor region 15 with a high impurity concentration comprising the source of the memory cell and an n^+-type semiconductor region 15 with a high impurity concentration comprising the source and drain of the n-channel type MISFET are formed by ion-implanting an n-type impurity (arsenic) to the p-type well 5 masked with a photoresist film with a

film thickness of about 1 μm where an opening is installed in the source forming region and the n-channel type MISFET forming region of the memory cell under a condition of acceleration energy 50 keV and dose amount $2\times10^{15}/cm^2$. Through the processes so far, the memory cell (MISFET Qm) and MISFET of the peripheral circuit (n-channel type MISFET Qn and p-channel type MISFET Qp) are completed.

[0074]

Next, as shown in Fig. 18, after accumulating a silicon oxide film 17 with a film thickness of about 500 nm on the semiconductor substrate 1 by the CVD method, contact holes 20, 21, and 22 are formed on the top of the drain of the memory cell, the top of the source and drain of the n-channel type MISFET Qn, and the top of the source and drain of the p-channel type MISFET Qp, respectively, by dry-etching the silicon oxide film 17 masked with a photoresist film.

[0075]

After that, an Al alloy film with a film thickness of about 500 nm is accumulated on the silicon oxide film 17 including the interiors of the contact holes 20~22 by the sputtering method, and wirings 23~27 are formed by patterning this Al alloy film by dry etching masked with a photoresist film, almost completing a flash memory of this embodiment shown in the Fig. 2.

[0076]

Because the flash memory of this embodiment configured in the above way has its memory cell made of a single MISFET in the same way as in the conventional floating gate type memory cell. The writing/erasing operation can be performed relatively easily, and it does not increase the necessary peripheral circuit area. Also, the manufacturing process becomes simple.

[0077]

Because the flash memory of this embodiment does not use high-resistance wiring at the reading operation such as the conventional memory cell equipped with side wall gate electrodes, no degradation in the reading speed occurs. Also, because it adopts a scheme where the gate electrode and drain are charged with a positive voltage and hot electrons generated near the source are injected to electron traps in a silicon nitride film at the writing operation, injection efficiency is improved as the potential difference between the source at the ground level and the gate electrode becomes large, enabling a lower-voltage operation than in the conventional cell structure.

[0078]

In the flash memory of this embodiment, because the gate electrodes of the memory cell cover the whole surface of the channel region, no parasitic resistance occurs immediately below the insulation film between the side wall gate electrode and the control gate electrode which is a problem in the conventional cell structure equipped with a side wall gate electrode, causing no decline in the drain current in the reading operation.

[0079]

In the flash memory manufacturing method of this embodiment, because the gate insulation film (three layers of insulation films consisting of silicon oxide film 7, silicon nitride film 8, and silicon

oxide film 9) in the source side of the memory cell is formed self-aligned to the gate electrode, it can be designed with the equivalent cell area to the conventional floating gate type memory cell, realizing nonvolatile memory excellent in scalability.

[0080]

(Embodiment 2)

A flash memory manufacturing method of this embodiment is explained using Fig. 19 ~ Fig. 33 (essential-section cross-sectional views of a semiconductor substrate each showing a part of the memory cell array region and its neighboring peripheral circuit region).

[0081]

First of all, as shown in Fig. 19, after forming a field oxide film 2 on the surface of a semiconductor substrate 1 made of a p-type silicon single crystal, a silicon oxide film 3 is formed on the surface of an element forming region surrounded with the field oxide film 2. Subsequently, after forming a deep n-type well 4 on the semiconductor substrate 1 in the memory cell array region, a shallow p-type well 5 is formed on the semiconductor substrate 1 in the memory cell array region and a part of the peripheral circuit (n-channel type MISFET forming region), and a shallow n-type well 6 is formed on the semiconductor substrate 1 in the other part of the peripheral circuit (p-channel type MISFET forming region). The processes so far are the same as in the embodiment 1.

[0082]

Next, as shown in Fig. 20, the semiconductor substrate 1 is thermally oxidized at about 800°C to form a gate oxide film 30 with a film thickness of about 15 nm on the surfaces of the p-type well 5 and the n-type well 6, afterwards as shown in Fig. 21, a polycrystalline silicon film (not shown in the figure) with a film thickness of about 200 is accumulated on the semiconductor substrate 1 by the thermal CVD method at about 600°C, and afterwards this polycrystalline silicon film 31 is dry-etched masked with a photoresist film, forming the gate electrode 31a of the memory cell and the gate electrodes 31b and 31c of the peripheral circuit.

[0083]

Next, as shown in Fig. 22, after accumulating a silicon nitride film 32 with a film thickness of about 20 nm on the semiconductor substrate 1 including the top portions of the gate electrodes 31a, 31b, and 31c by the CVD method, a silicon oxide film 33 with a film thickness of about 50 nm is accumulated on the top of the silicon nitride film 32 by the CVD method.

[0084]

Next, as shown in Fig. 23, a silicon oxide film 33 is wet-etched masked with a photoresist film with a film thickness of about 1 μm where openings are installed in the source forming region of the memory cell and its vicinity. Subsequently the photoresist film is removed by ashing, and afterwards the silicon nitride film 32 covering the source forming region of the memory cell and the gate electrode 31a in its vicinity is removed by wet-etching the silicon nitride film 32 masked with the silicon oxide film 33.

[0085]

Next, as shown in Fig. 24, the gate oxide film covering the source forming region of the memory cell is removed by wet-etching masked with the silicon nitride film 32. At this time, the gate oxide film 30 in the lower part of the gate electrode 31, a pattern-formed next to the source forming region is also etched, and a part of it is undercut over about 70 nm in width from its edge.

[0086]

Next, as shown in Fig. 25, the semiconductor substrate 1 is thermally oxidized at about 750°C to form a silicon oxide film 34 with film thickness of about 5 nm on the source forming region of the memory cell and the surface of the p-type well 5 exposed in the vicinity. At this time, the gate electrode 31a exposed in the vicinity of the source forming region of the memory cell, is also oxidized at the same time, forming a silicon oxide film 35 with film thickness of about 5 nm on its surface.

[0087]

Next, as shown in Fig. 26, a silicon nitride film 36 with film thickness of about 10 nm is accumulated on the semiconductor substrate 1 by the CVD method. By this, three layers of gate insulation film consisting of the silicon oxide film 34, silicon nitride film 36, and silicon oxide film 35 are formed in the source forming region side in the lower part of the gate electrode 10a.

[0088]

Next, as shown in Fig. 27, the n^--type semiconductor regions 37 with a low impurity concentration are formed on the p-type well 5 on both sides of each of the gate electrodes 10a and 10c and the n-type well 6 on both sides of the gate electrode 10b by ion-implanting a n-type impurity (phosphorus) to the whole surface of the semiconductor substrate 1 under a condition of acceleration energy 40 keV and dose amount $1\times10^{13}/cm^2$.

[0089]

Next, as shown in Fig. 28, an n^+-type semiconductor region 39 comprising the drain of the memory cell is formed by ion-implanting a n-type impurity (arsenic) to the p-type well 5 masked with a photoresist film with a film thickness of about 1 μm where an opening is installed in the drain forming region of the memory cell under a condition of acceleration energy 50 keV and dose amount $3\times10^{15}/cm^2$.

[0090]

Next, as shown in Fig. 29, a p^--type semiconductor region 38 with a low impurity concentration is formed through compensating the n^--type semiconductor region 37 to the n-type well 6 on both sides of the gate electrode 31b by ion-implanting a p-type impurity (boron difluoride) to the n-type well 6 masked with a photoresist film with a film thickness of about 1 μm where an opening is installed in the p-channel type MISFET forming region under a condition of acceleration energy 50 keV and dose amount $2\times10^{13}/cm^2$.

[0091]

Next, as shown in Fig. 30, after accumulating a silicon oxide film with a film thickness of about 200 nm on the semiconductor substrate 1 by the CVD method, a side wall spacer 42 of about 150 nm in

width is formed on side wall of each of the gate electrodes 31a, 31b, and 31c by etching anisotropically this silicon oxide film. At this time, the silicon oxide film 35 and the silicon nitride film 36 covering the upper parts of the gate electrodes 31a, 31b, and 31c are also etched at the same time, exposing the surfaces of the gate electrodes 31a, 31b, and 31c.

[0092]

Next, as shown in Fig. 31, a p^+-type semiconductor region 40 with a high impurity concentration comprising the source and drain of the p-channel type MISFET is formed by ion-implanting a p-type impurity (boron difluoride) to the n-type well 6 masked with a photoresist film with a film thickness of about 1 μm where an opening is installed in the p-channel type MISFET forming region under a condition of acceleration energy 50 keV and dose amount $3\times10^{15}/cm^2$.

[0093]

Subsequently, an n^+-type semiconductor region 41 with a high impurity concentration comprising the source of the memory cell and an n^+-type semiconductor region 41 with a high impurity concentration comprising the source and drain of the n-channel type MISFET are formed by an ion-implanting n-type impurity (arsenic) to the p-type well 5 masked with a photoresist film with a film thickness of about 1 μm where an opening is installed in the source forming region and the n-channel type MISFET forming region of the memory cell under a condition of acceleration energy 50 keV and dose amount $2\times10^{15}/cm^2$. Through the processes so far, the memory cell (MISFET Qm) and MISFET of the peripheral circuit (n-channel type MISFET Qn and p-channel type MISFET Qp) are completed.

[0094]

Next, after removing he silicon oxide film 34 covering the surfaces of the source and drain of the MISFET by etching the surface of the semiconductor substrate 1, as shown in Fig. 32, silicide layers 43 of low resistance are formed on the surfaces of the gate electrodes 31a, 31b, and 31c and the source and drain (n^+-type semiconductor region 39, p^+-type semiconductor region 40, and n^+-type semiconductor region 41). The silicide layer 43 is formed, for example, by accumulating a high melting point metal film such as Co (cobalt) film and Ti (cobalt) film by the sputtering method, next thermally processing the semiconductor substrate 1 to react the high melting point metal film with the substrate (Si) and the gate electrodes (31a~31c) forming a Co silicide layer, and removing the unreacted high melting point metal film by wet etching.

[0095]

Next, as shown in Fig. 33, in the same way as in embodiment 1, after forming contact holes 45, 46, and 47 on a silicon oxide film 44 accumulated on the semiconductor substrate 1, wirings 48~52 are formed on the top of the silicon oxide film 44, almost completing the flash memory of this embodiment 2.

[0096]

Figure 34 is a table listing the photomasks used in the manufacturing method. Among the thirteen photomasks used in the metal manufacturing process, the photomasks proper to manufacture memory cell are two pieces of one (No. 6) for processing silicon nitride film and another (No. 7) for drain formation, being very simplified.

[0097]

Also, the writing/erasing operation property and retention property of the flash memory manufactured in the method were in the same degrees with those of the flash memory of the embodiment 1.

[0098]

(Embodiment 3)

Figure 35 is an essential-section cross-sectional view of a semiconductor substrate showing the cell structure of a flash memory of this embodiment.

[0099]

While the drain-side gate insulation film is composed of one layer of silicon oxide film 9 in the memory cell (MISFET Qm) of embodiment 1, in this embodiment the drain-side gate insulation film is composed of two layers of the silicon oxide film 9 and silicon oxide film 60 formed underneath. Also, the electric capacity film thickness of the drain-side gate insulation film consisting of these two layers of silicon oxide film 9 and 60 is approximately equal to the electric capacity film thickness of the source-side gate insulation film composed of the silicon oxide film 7 and 9 and a silicon nitride film 8 sandwiched between them. Namely, the gate insulation film of this memory cell consists of almost the same electric capacity film thickness (about 17.5 nm for example) in the drain side and source side.

[0100]

The configuration and program operation of the memory cell of this embodiment, except as described above, are the same as those of the memory cell of embodiment 1. Also, the memory cell manufacturing method of this embodiment is the same as the manufacturing method in embodiment 1, except that one process increases, where the silicon oxide film 60 is formed by thermally processing the semiconductor substrate 1.

[0101]

According to the flash memory of this embodiment, by setting the electric capacity film thickness of the gate insulation film about the same over the entire lower part of the gate electrode 10a, even when the length of the source-side gate insulation film (silicon oxide film 9, silicon nitride film 8, and silicon oxide 7) along the gate length direction varies due to a variation in the manufacturing process, the drain current driving capability will not change. By this, because the drain current at the writing operation becomes constant, a variation of writing time is prevented, and a stable memory cell property becomes possible.

[0102]

(Embodiment 4)

Figure 36 is an essential-section cross-sectional view of a semiconductor substrate showing the cell structure of a flash memory of this embodiment.

[0103]

While only the source-side gate insulation film is composed of a three-layer film (silicon oxide film 9, silicon nitride film 8, and silicon oxide film 7), in this embodiment the whole drain-side gate insulation film in the lower part of the gate electrode 10a is composed of the three-layer film (silicon oxide film 9, silicon nitride film 8, and silicon oxide film 7). The film thickness of these three layers total about 7 nm.

[0104]
The configuration and program operation of the memory cell of this embodiment other than those differences described above are the same as the memory cell of embodiment 1. Also, the memory cell manufacturing method of this embodiment is the same as the manufacturing method described in embodiment 1, except that one process is omitted where the silicon oxide film 7 and silicon nitride film 8 are patterned to leave them only in the source side. This memory cell was written at 1 μ/sec.

[0105]

(Embodiment 5)

Figure 37 is an essential-section cross-sectional view of a semiconductor substrate showing the cell structure of a flash memory of this embodiment.

[0106]

This flash memory cell is composed with the MISFET Qc which is a memory element section and the selection MISFET Qs. The MISFET Qc in the memory element section mainly consists of a writing/erasing gate electrode (PEG) 73 made of a polycrystallne silicon film formed on a gate insulation film with three-layer structure consisting of a bottom gate oxide film 70 with a film thickness of about 8 nm, a silicon nitride film 71 with a film thickness of about 10 nm, and a top gate oxide film 72 with a film thickness of about 10 nm, etc. and a source and a drain (connecting diffusion layer) formed on a semiconductor substrate 1 on both sides of this gate electrode 73.

[0107]

The source consists of an n^--type semiconductor region 74 with a low impurity concentration whose one end extends to the bottom of the gate electrode 73 and an n^+-type semiconductor region with a high impurity concentration formed so that it is offset relative to the gate electrode 73, and the drain (connecting diffusion layer) consists of an n^+-type semiconductor region 76 whose one end extends to the bottom of the gate electrode 73.

[0108]

Also, the selection MISFET Qs mainly consists of a selection gate electrode (SG) 78 made of a polycrystalline silicon film etc. formed on the top of the gate oxide film 77 with a film thickness of about 4 nm, a source (connecting diffusion layer) and a drain formed on the semiconductor substrate 1 on both sides of this gate electrode 78. The drain consists of an n^--type semiconductor region 79 with a high impurity concentration whose one end extends to the bottom of the gate electrode 78. The source consists of an n^+-type semiconductor region 76 which is the drain of the MISFET Qc, and its one end extends to the bottom of the gate electrode 78.

[0109]

The program operations of the flash memory is explained using Fig. 38 (a memory cell operation voltage table). Writing is performed by charging the drain of the selection MISFET Qs with 5 V, the gate electrode 78 with 2 V, turning the selection MISFET Qs on, charging the gate electrode 73 with 5 V with the source of the MISFET Qc of the memory element section as the ground level (0 V), and a peak in the electric field intensity is generated near an n^--type semiconductor region 74 with a low impurity concentration comprising a part of the source. By this, hot electrons generated in this region are injected to the electron traps inside the silicon nitride film 71, the threshold voltage seen from the gate electrode 73 of the MISFET Qc rises to 4 V or higher, and writing is performed. Because this memory cell can control the drain current with the voltage charged to the gate electrode 73, compared with the conventional MNOS-type memory cell where electrons are injected to the whole surface of a silicon nitride film from the substrate side via a direct tunnel oxide film by controlling the potential of the substrate and writing/erasing gate electrode, writing can be performed with lower electric power consumption.

[0110]

The erasing operation is performed by charging the gate electrode 73 of the MISFET Qc with −10 V and the source and well with 5 V, and ejecting electrons inside the silicon nitride film 71. Also, the writing operation is performed by charging the drain gate electrode 73 of the selection MISFET Qs and the gate electrode 73 of the MISFET Qc with 2 V, and judging the threshold voltage of the MISFET Qc.

[0111]

(Embodiment 6)

Figure 39 is an essential-section cross-sectional view of a semiconductor substrate showing the cell structure of a flash memory of this embodiment.

[0112]

The MISFET comprising this memory cell mainly consists of a gate electrode 83 made of a polycrystalline silicon film etc. formed on a gate insulation film, and a source and a drain formed on a semiconductor substrate 1 on both sides of this gate electrode 83. The source consists of an n^+-type semiconductor region 84 with a high impurity concentration whose one end extends to the lower part of the gate electrode 83, and the drain consists of a p^--type semiconductor region 85 with a low impurity concentration (about 1×10^{18}~$10^{19}/cm^3$) whose one end extends to the lower part of the gate electrode 83 and an n^+-type semiconductor region 86 with a high impurity concentration formed offset relative to the gate electrode 83. Also, in the gate insulation film, while the source side consists of a gate oxide 82 with a film thickness of about 10 nm, the drain size consists of a bottom gate oxide film 80 with a film thickness of about 8 nm, a silicon nitride film 81 with a film thickness of about 10 nm, and a top gate oxide film 82 with a film thickness of about 10 nm. In this way, the memory cell of this embodiment has a characteristic in that it performs the injection of hot electrons at the time of writing in the drain side.

[0113]

As shown in Fig. 40, the writing and erasing operations of this flash memory are the same as in the memory cell of embodiment 1. On the other hand, writing is performed by charging each of the gate electrode 83 and the source with a positive voltage of 5 V with the drain of the selected memory cell as the ground level (0 V).

[0114]

Figure 41 is a plot showing time change of the voltage charged to each terminal at the writing operation. Writing is performed by pre-charging all the bit lines to 5 V after charging the common source line of the selected memory block with 5 V. Next, after raising the potential of only the selected word line to 5 V, only the selected bit line is lowered to 0 V. This time for lowering it to 0 V is the writing time, and a channel current flows from the source to drain direction of the memory cell within this time. At this time, as shown in Fig. 42, because most of the potential levels set to 5 V in the source side and 0 V in the drain side drop in the low concentration drain (p^--type semiconductor region 85) region, a peak of the electric field intensity occurs at the edge of the drain. Then, hot electrons generated by this high electric field are accelerated by the transverse direction electric field of 5 V charged to the selected word line and injected to the electron traps inside the silicon nitride film 81, thus performing writing.

[0115]

(Embodiment 7)

Figure 43 is an essential-section cross-sectional view of a semiconductor substrate showing the cell structure of a flash memory of this embodiment.

[0116]

This memory cell performs the injection of hot electrons at the writing time in the drain side and has the same cell structure as embodiment 6 except that the source consists of an n^--type semiconductor region 87 with a low impurity concentration whose one end extends to the lower part of the gate electrode 83 and an n^+-type semiconductor region 84 with a high impurity concentration formed offset relative to the gate electrode 83.

[0117]

Writing is started by pre-charging all the bit lines to 5 V after charging the common source line of the selected memory block to 5 V in the same way as embodiment 6. By the way, if this 5 V power supply for writing is an internal power supply such as a booster circuit formed on a chip, because the power supply capability is limited, there occurs a problem that charging to a large enough voltage becomes impossible if there is a large connection leak of the current of the common source line to be charged. In this embodiment, by forming an n^--type semiconductor region 87 with a low impurity concentration in the source side, because the electric field of the source connection is moderated when charging the source at the writing time. The problem can be avoided by attempting a reduction of the leak current and an improvement of the connection voltage resistance of the source connection.

[0118]

(Embodiment 8)

Figure 44 is an outline plan showing the cell structure of a flash memory of this embodiment, and Fig. 45 is a essential-section cross-sectional view of the semiconductor substrate along the A-A' line in Fig. 44.

[0119]

In the MISFET Qm comprising the memory cell of this embodiment, in the same way as embodiment 1, the source-side gate insulation film consists of a three-layer film (silicon oxide film 9, silicon nitride film 8, and silicon oxide film 7), and the drain side consists of a one layer of silicon oxide film 9. On the other hand, the bit lines DL and the drain (n^+-type semiconductor region 92) are electrically connected via a plug 98 formed on the upper part of the drain. Also, the sources (n^+-type semiconductor region 92) of a plurality of memory cells along the extending direction of the gate electrode 90 are electrically connected via the source lines (SL) consisting of plug 98 formed on their top.

[0120]

In order to manufacture the memory cell, first as shown in Fig. 46, after a deep n-type well 4 and a shallow p-type well 5 are formed on a p-type semiconductor substrate 1 by the same method as in embodiment 1, a gate insulation film whose source side consists of a three-layer film (silicon oxide film 9, silicon nitride film 8, and silicon oxide film 7) and drain side consists of one layer of silicon oxide film 9 is formed on the surface of the p-type well 5.

[0121]

The silicon oxide film 7 is formed by thermally oxidizing the semiconductor substrate 1 at about 800°C, and its film thickness is set to about 11 nm. Also, the silicon nitride film 8 is formed by the thermal CVD method at about 730°C, and its film thickness is set to about 10 nm. Moreover, the silicon oxide film 9 is formed by patterning the silicon nitride film 8 and silicon oxide film 7 to leave these films only on the source forming region of the memory cell and its vicinity, and then thermally oxidizing the semiconductor substrate 1 at about 800°C, and its film thickness is set to about 15 nm.

[0122]

Next, as shown in Fig. 47, a polycrystalline silicon film with a film thickness of about 100 nm and phosphorus concentration of about $2\times10^{20}/cm^3$ is accumulated on the top of the silicon oxide film 9 by the CVD method, and next after accumulating a silicon nitride film 93 with a film thickness of about 200 nm on the top by the CVD method, these films are patterned by dry etching masked with a photoresist film, forming a gate electrode 90 consisting of the polycrystalline silicon film.

[0123]

Next, as shown in Fig. 48, a p^--type semiconductor region 91 is formed by ion-implanting a p-type impurity (boron) to the p-type well 5 from an oblique 30° angle masked with a photoresist film where an opening is installed in the source forming region under a condition of acceleration energy 20 keV and dose amount $1\times10^{13}/cm^2$. Subsequently, an n+-type semiconductor region 92 comprising the source and drain is formed on the p-type well 5 on both sides of the gate electrode 90 by an ion-implanting n-type impurity (arsenic) to the whole surface of the memory cell array region under a condition of acceleration energy 50 keV and dose amount $2\times10^{15}/cm^2$.

[0124]

Next, as shown in Fig. 49, after accumulating a silicon nitride film on the semiconductor substrate 1 by the CVD method, by anisotropically etching this silicon nitride film, a side wall spacer 94 is formed on the side wall of the gate electrode 90. At this time, the gate insulation film covering the surfaces of the source and drain is etched at the same time.

[0125]

Next, as shown in Fig. 50, after accumulating a silicon oxide film 95 on the semiconductor substrate 1 by the CVD method, by etching this silicon oxide film 95 masked with a photoresist film where an opening is installed on the upper part of the drain, a contact hole 96 is formed in the source line forming region including the upper part of the source, and a contact hole 97 is formed on the upper part of the drain.

[0126]

In the process of etching the silicon oxide film 95, because the side wall spacer 94 of silicon nitride formed on the side wall, the gate electrode 90 functions as an etching stopper, the contact holes 96 and 97 are formed self-aligned to the space of the gate electrode 90. By this, because the fitting allowance between the contact holes 96 and 97 and the gate electrode 90 becomes unnecessary, the space of the gate electrode 90 can be designed in the minimum processing size.

[0127]

Next, as shown in Fig. 91, source lines (SL) are formed inside the contact hole 96, and a plug 98 is formed inside the contact hole 97. The source lines (SL) and the plug 98 are formed by accumulating a polycrystalline silicon film doped with an n-type impurity on the top of the silicon oxide film 95 by the CVD method and then flattening the surface of this polycrystalline silicon film by the chemical-mechanical polishing (CMP) method.

[0128]

Subsequently, after accumulating a silicon oxide film 99 on the top of the silicon oxide film 95 by the CVD method, an Al alloy film is accumulated on the top of the silicon oxide film 99 by the sputtering method, and by patterning this Al alloy film by dry etching masked with a photoresist film to form bit lines DL, the flash memory of this embodiment shown in the Fig. 44 and Fig. 45 is almost completed.

[0129]

According to this embodiment, because the space of the gate electrode 90 can be designed with the minimum processing size, the cell area could be reduced to 0.5 $\mu m \times 0.4\ \mu m = 0.2\ \mu m^2$ at the gate length of 0.3 μm. Also, writing time of the memory cell was 5 microseconds and the erasing time was 10 milliseconds, confirming enough stable retention property similar to the embodiment 1.

[0130]

Above, although the invention made by the present inventors was explained concretely based on the embodiments, this invention is not limited to the embodiments but can be changed in various ways within the range not deviating from its essence.

[0131]

Because the nonvolatile memory of this invention has a simple cell structure and a simple manufacturing process, application to LSIs where nonvolatile memory and logic LSI are mounted on the same semiconductor substrate is also easy.

[0132]

[Efficacy of the Invention]

Among the inventions disclosed in this application, the effects obtained by the representative ones are simply explained below.

[0133]

In the nonvolatile memory of this invention, because the memory cell consists of a single MISFET, writing/erasing operation can be performed relatively easily, not increasing the necessary peripheral circuit area. Also, its manufacturing process is simple.

[0134]

Because the nonvolatile memory of this invention adopts a scheme where a positive voltage is charged to the gate electrode and drain at the writing operation and hot electrons generated near the source are injected to the electron traps inside the silicon nitride film, the potential difference between the source at the ground level and the gate electrode becomes large, improving the injection efficiency and enabling operation at a lower voltage compared with the conventional cell structure.

[0135]

In the nonvolatile memory manufacturing method of this invention, because the source-side gate insulation film (a three-layer insulation film consisting of silicon oxide film, silicon nitride film, and silicon oxide film) of the memory cell is formed self-aligned to the gate electrode, it can be designed to have the equivalent cell area to the conventional floating gate type memory cell, realizing nonvolatile memory excellent in scalability.

[Brief Explanation of the Drawings]

[Fig. 1]

An outline circuit diagram showing the main section of the flash memory which is embodiment 1 of this invention.

[Fig. 2]

A cross-sectional view showing the essential section of the flash memory which is embodiment 1 of this invention.

[Fig. 3A]

A plan view showing the conductive layer pattern of the flash memory which is embodiment 1 of this invention.

[Fig. 3B]

A plan view showing the conductive layer pattern of the flash memory which is embodiment 1 of this invention.

[Fig. 4]

An outline cross-sectional view explaining the program operation of the flash memory which is embodiment 1 of this invention.

[Fig. 5]

An operation voltage table explaining the program operation of the flash memory which is embodiment 1 of this invention.

[Fig. 6]

A plot showing the potential distribution and electric field intensity distribution in the channel region in the writing operation of the flash memory which is embodiment 1 of this invention.

[Fig. 7]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 8]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 9]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 10]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 11]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 12]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 13]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 14]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 15]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 16]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 17]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 18]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 1 of this invention.

[Fig. 19]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 20]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 21]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 22]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 23]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 24]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 25]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 26]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 27]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 28]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 29]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 30]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 31]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 32]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 33]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 34]

A flow chart showing the manufacturing method of the flash memory which is embodiment 2 of this invention.

[Fig. 35]

An outline cross-sectional view of the flash memory which is embodiment 3 of this invention.

[Fig. 36]

An outline cross-sectional view of the flash memory which is embodiment 4 of this invention.

[Fig. 37]

An outline cross-sectional view of the flash memory which is embodiment 5 of this invention.

[Fig. 38]

An operation voltage table explaining the program operation of the flash memory which is embodiment 5 of this invention.

[Fig. 39]

An outline cross-sectional view of the flash memory which is embodiment 6 of this invention.

[Fig. 40]

An operation voltage table explaining the program operation of the flash memory which is embodiment 6 of this invention.

[Fig. 41]

A plot showing the time change of charged voltage in the writing operation of the flash memory which is embodiment 6 of this invention.

[Fig. 42]

A plot showing the potential distribution and electric field intensity distribution of the channel region in the writing operation of the flash memory which is embodiment 6 of this invention.

[Fig. 43]

An outline cross-sectional view of the flash memory which is embodiment 7 of this invention.

[Fig. 44]

An essential-section cross-sectional view showing the cell structure of the flash memory which is embodiment 8 of this invention.

[Fig. 45]

An essential-section cross-sectional view of the semiconductor substrate along the A-A' line in Fig. 44.

[Fig. 46]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 8 of this invention.

[Fig. 47]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 8 of this invention.

[Fig. 48]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 8 of this invention.

[Fig. 49]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 8 of this invention.

[Fig. 50]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 8 of this invention.

[Fig. 51]

An essential-section cross-sectional view showing the manufacturing method of the flash memory which is embodiment 8 of this invention.

[Fig. 52]

An outline cross-sectional view showing the cell structure of a floating gate type memory cell.

[Fig. 53]

An outline cross-sectional view showing the cell structure of an MNOS-type memory cell.

[Fig. 54]

An outline cross-sectional view showing the cell structure of a memory cell having a selection gate electrode and a side wall gate electrode.

[Fig. 55]

A plot showing the potential distribution and electric field intensity distribution of the channel region in the writing operation of the flash memory shown in Fig. 54.

[Explanation of the Codes]

1: Semiconductor substrate
2: Field oxide film
3: Silicon oxide film
4: (Deep) n-type well
5: p-type well
6: n-type well
7: Silicon oxide film
8: Silicon nitride film
9: Silicon oxide film
10a, 10b, 10c: Gate electrodes
11: n^--type semiconductor region
12: p^--type semiconductor region
13: n^+-type semiconductor region
14: p^+-type semiconductor region
15: n^+-type semiconductor region
16: Side wall spacer
17: Silicon oxide film
20~22: Contact holes
23~27: Wirings
30: Gate oxide film
31a, 31b, 31c: Gate electrodes
32: Silicon nitride film
33: Silicon oxide film
34: Silicon oxide film
35: Silicon oxide film
36: Silicon nitride film
37: n^--type semiconductor region
38: p^--type semiconductor region
39: n^+-type semiconductor region
40: p^+-type semiconductor region
41: n^+-type semiconductor region
42: Side wall spacer

43: Silicide film
44: Silicon oxide film
45~47: Contact holes
48~52: Wiring 60 Silicon oxide film
70: Bottom gate oxide film
71: Silicon nitride film
72: Top gate oxide film
73: Gate electrode
74: n^--type semiconductor region
75: n^+-type semiconductor region
76: n^+-type semiconductor region
77: Gate oxide film
78: Gate electrode
79: n^+-type semiconductor region
80: Bottom gate oxide film
81: Silicon nitride film
82: (Top) Gate oxide film
83: Gate electrode
84: n^--type semiconductor region
85: p^--type semiconductor region
86: n^+-type semiconductor region
87: n^--type semiconductor region
90: Gate electrode
91: p^--type semiconductor region
92: n^+-type semiconductor region (source, drain)
93: Silicon nitride film (cap)
94: Side wall spacer
95: Silicon oxide film
96, 97: Contact holes
98: Plug
99: Silicon oxide film
101: Silicon substrate
102: Gate oxide film
103: Floating gate
104: Interlayer insulation film
105: Control gate
106: Source
107: Drain
108: Electron
111: Silicon substrate
112: Direct tunnel oxide film
113: Silicon nitride film
114: Gate oxide film
115a, 115b: Gate electrode
116: Source
117: Connecting diffusion layer drain
118: Gate oxide film
119: Drain
121: Silicon substrate
122: Gate oxide film

123: Selection gate electrode
124: Silicon oxide film
125: Silicon nitride film
126: Silicon oxide film
127: Side wall gate electrode
128: Source
129: Drain
CSL: Common source line
DL (DL1~DLn): Bit lines
MA: Memory cell array
M (M11~Mnm): Memory cells
Qc: MISFET
Qm: MISFET
Qs: Selection MISFET
SL (SL1~SLm/2): Source lines
SA: Sense amplifier
WL (WL1~WLm): Word lines
X-DEC: Low decoder
Y-DEC: Column decoder

[Abstract]

[Objective]

The objective of this invention is to provide a nonvolatile memory equipped with a new cell structure having both scalability comparable to the floating gate type memory cell and reliability equivalent to or higher than the MNOS-type memory cell and its manufacturing method.

[Resolution Means]

The MISFET Qm comprising nonvolatile memory consists of a gate electrode 10a formed on the gate insulation film, an n^+-type semiconductor region 13 (drain) whose one end extends to the bottom of a gate electrode 10a, an n^+-type semiconductor region 15 (high concentration source) formed offset relative to the gate electrode 10a, and an n^--type semiconductor region 11 (low concentration source) whose one end extends to the bottom of the gate electrode 10a. In the gate insulation film, the drain side consists of one layer of silicon oxide film 9, the source side consists of three layers of insulation films where a silicon oxide film 7, a silicon nitride film 8, and a silicon oxide film 9 are accumulated.

[Fig. 5]

Terminal	Bit lines (Drain voltage)		Word lines (Gate voltage)		Source lines	Well
	Select	Deselect	Select	Deselect		
Write	5 V	0 V	5 V	0 V	0 V	0 V
Erase	0 V	0 V	-10 V	0 V	5 V	5 V
Read	2 V	0 V	2 V	0 V	0 V	0 V

[Fig. 34]
1. Isolation formation
2. Deep n-type well implantation
3. Shallow n-type well implantation

4. p-type well implantation
5. Gate electrode processing
8. Peripheral pMOS low concentration source & drain implantation
9. n^+-type semiconductor region implantation
10. p^+-type semiconductor region implantation
11. Contact hole opening
12. First metal wiring processing

[Fig. 38]

Terminal	Bit lines (D)		Word lines (SG)		Write/Erase lines (PEG)		Source lines (S)	Well
	Select	Deselect	Select	Deselect	Select	Deselect		
Write	5 V	0 V	2 V	0 V	5 V	0 V	0 V	0 V
Erase	0 V	0 V	0 V	0 V	-10 V	0 V	5 V	5 V
Read	2 V	0 V	2 V	0 V	2 V	0 V	0 V	0 V

[Fig. 40]

Terminal	Bit lines (Drain voltage)		Word lines (Gate voltage)		Source lines	Well
	Select	Deselect	Select	Deselect		
Write	0 V	5 V	5 V	0 V	5 V	0 V
Erase	0 V	0 V	-10 V	0 V	5 V	5 V
Read	2 V	0 V	2 V	0 V	0 V	0 V

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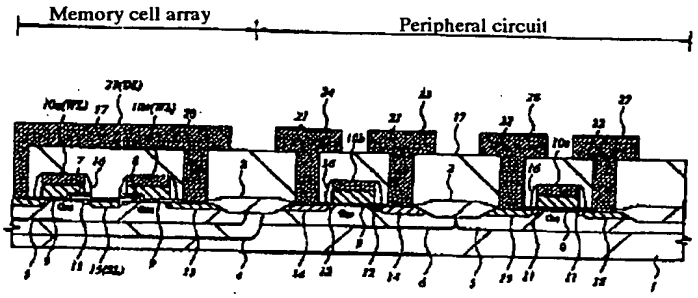
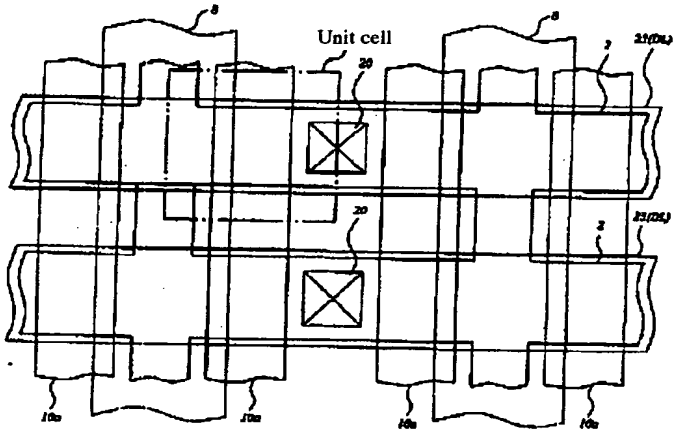
(58) Investigated Fields (Int. Cl.[6], DB name)

H01L 27/115
H01L 21/8247
H01L 29/788
H01L 29/792

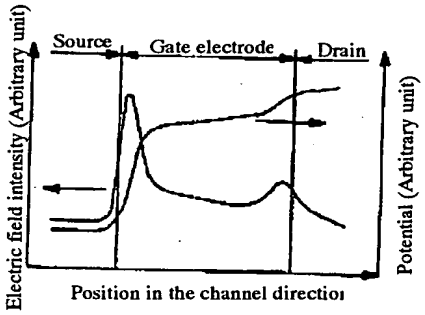
[Fig. 2]

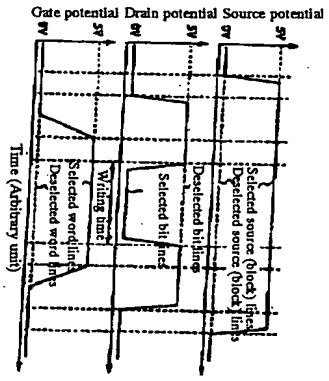


[Fig. 3A]

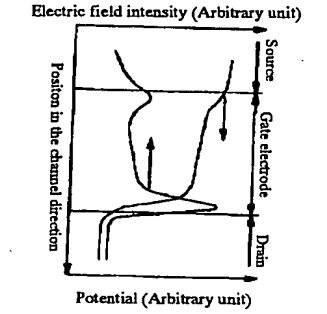


[Fig. 6]


Source
Gate electrode
Drain
Electric field intensity (Arbitrary unit)
Potential (Arbitrary unit)
Position in the channel direction

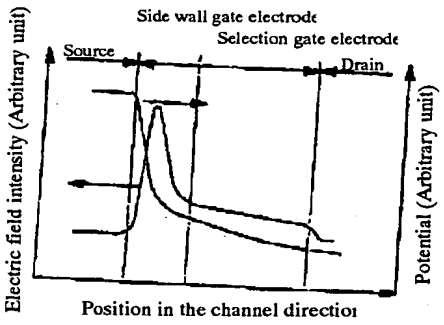

Gate potential
Drain potential
Source potential
5V
5V
0V
5V
0V
5V
Time (Arbitrary unit)
Selected word line
Deselected word lines
Writing time
Selected bit line
Deselected bit line
Selected source (block) lines
Deselected source (block) lines

[Fig. 41]


Electric field intensity (Arbitrary unit)
Position in the channel direction
Source
Gate electrode
Drain
Potential (Arbitrary unit)

[Fig. 42]

[Fig. 55]


Side wall gate electrode
Selection gate electrode
Source
Drain
Electric field intensity (Arbitrary unit)
Potential (Arbitrary unit)
Position in the channel direction